# NSS40200UW6T1G

# 40 V, 4.0 A, Low $V_{CE(sat)}$ PNP Transistor

ON Semiconductor's $e^2$PowerEdge family of low $V_{CE(sat)}$ transistors are miniature surface mount devices featuring ultra low saturation voltage ($V_{CE(sat)}$) and high current gain capability. These are designed for use in low voltage, high speed switching applications where affordable efficient energy control is important.

Typical applications are DC−DC converters and power management in portable and battery powered products such as cellular and cordless phones, PDAs, computers, printers, digital cameras and MP3 players. Other applications are low voltage motor controls in mass storage products such as disc drives and tape drives. In the automotive industry they can be used in air bag deployment and in the instrument cluster. The high current gain allows $e^2$PowerEdge devices to be driven directly from PMU's control outputs, and the Linear Gain (Beta) makes them ideal components in analog amplifiers.

- This is a Pb−Free Device

**MAXIMUM RATINGS** ($T_A$ = 25°C)

| Rating | Symbol | Max | Unit |
|---|---|---|---|
| Collector-Emitter Voltage | $V_{CEO}$ | −40 | Vdc |
| Collector-Base Voltage | $V_{CBO}$ | −40 | Vdc |
| Emitter-Base Voltage | $V_{EBO}$ | −7.0 | Vdc |
| Collector Current − Continuous | $I_C$ | −2.0 | Adc |
| Collector Current − Peak | $I_{CM}$ | −4.0 | A |
| Electrostatic Discharge | ESD | HBM Class 3B<br>MM Class C | |

**THERMAL CHARACTERISTICS**

| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Total Device Dissipation, $T_A$ = 25°C<br>Derate above 25°C | $P_D$ (Note 1) | 875<br>7.0 | mW<br>mW/°C |
| Thermal Resistance,<br>Junction−to−Ambient | $R_{\theta JA}$ (Note 1) | 143 | °C/W |
| Total Device Dissipation, $T_A$ = 25°C<br>Derate above 25°C | $P_D$ (Note 2) | 1.5<br>11.8 | W<br>mW/°C |
| Thermal Resistance,<br>Junction−to−Ambient | $R_{\theta JA}$ (Note 2) | 85 | °C/W |
| Thermal Resistance,<br>Junction−to−Lead #1 | $R_{\theta JL}$ (Note 2) | 23 | °C/W |
| Total Device Dissipation<br>(Single Pulse < 10 sec) | $P_{Dsingle}$<br>(Notes 2 & 3) | 3.0 | W |
| Junction and Storage<br>Temperature Range | $T_J$, $T_{stg}$ | −55 to<br>+150 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. FR−4 @ 100 mm$^2$, 1 oz copper traces.
2. FR−4 @ 500 mm$^2$, 1 oz copper traces.
3. Thermal response.

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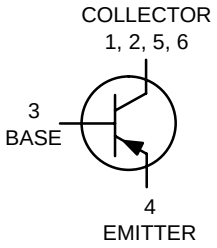
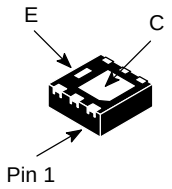
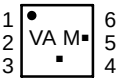
## −40 VOLTS
## 4.0 AMPS
## PNP LOW $V_{CE(sat)}$ TRANSISTOR
## EQUIVALENT $R_{DS(on)}$ 100 mΩ




**WDFN6**
**CASE 506AP**

**MARKING DIAGRAM**




VA = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| NSS40200UW6T1G | WDFN6<br>(Pb−Free) | 3000/<br>Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Collector−Emitter Breakdown Voltage ($I_C$ = −10 mAdc, $I_B$ = 0) | $V_{(BR)CEO}$ | −40 | − | − | Vdc |
| Collector−Base Breakdown Voltage ($I_C$ = −0.1 mAdc, $I_E$ = 0) | $V_{(BR)CBO}$ | −40 | − | − | Vdc |
| Emitter−Base Breakdown Voltage ($I_E$ = −0.1 mAdc, $I_C$ = 0) | $V_{(BR)EBO}$ | −7.0 | − | − | Vdc |
| Collector Cutoff Current ($V_{CB}$ = −40 Vdc, $I_E$ = 0) | $I_{CBO}$ | − | − | −0.1 | μAdc |
| Emitter Cutoff Current ($V_{EB}$ = −7.0 Vdc) | $I_{EBO}$ | − | − | −0.1 | μAdc |
| **ON CHARACTERISTICS** | | | | | |
| DC Current Gain (Note 4)<br>($I_C$ = −10 mA, $V_{CE}$ = −2.0 V)<br>($I_C$ = −500 mA, $V_{CE}$ = −2.0 V)<br>($I_C$ = −1.0 A, $V_{CE}$ = −2.0 V)<br>($I_C$ = −2.0 A, $V_{CE}$ = −2.0 V) | $h_{FE}$ | <br>150<br>150<br>150<br>150 | <br>−<br>−<br>−<br>− | <br>−<br>−<br>−<br>− | |
| Collector−Emitter Saturation Voltage (Note 4)<br>($I_C$ = −0.1 A, $I_B$ = −0.010 A) (Note 5)<br>($I_C$ = −1.0 A, $I_B$ = −0.100 A)<br>($I_C$ = −1.0 A, $I_B$ = −0.010 A)<br>($I_C$ = −2.0 A, $I_B$ = −0.020 A) | $V_{CE(sat)}$ | <br>−<br>−<br>−<br>− | <br>−<br>−0.100<br>−<br>− | <br>−0.020<br>−0.120<br>−0.200<br>−0.300 | V |
| Base−Emitter Saturation Voltage (Note 4)<br>($I_C$ = −1.0 A, $I_B$ = −0.01 A) | $V_{BE(sat)}$ | − | −0.76 | −0.900 | V |
| Base−Emitter Turn−on Voltage (Note 4)<br>($I_C$ = −2.0 A, $V_{CE}$ = −3.0 V) | $V_{BE(on)}$ | − | −0.80 | −0.900 | V |
| Cutoff Frequency<br>($I_C$ = −100 mA, $V_{CE}$ = −5.0 V, f = 100 MHz) | $f_T$ | 140 | − | − | MHz |
| Input Capacitance ($V_{EB}$ = −0.5 V, f = 1.0 MHz) | Cibo | − | | 500 | pF |
| Output Capacitance ($V_{CB}$ = −3.0 V, f = 1.0 MHz) | Cobo | − | | 100 | pF |
| **SWITCHING CHARACTERISTICS** | | | | | |
| Delay ($V_{CC}$ = 30 V, $I_C$ = 750 mA, $I_{B1}$ = 15 mA) | $t_d$ | − | − | 70 | ns |
| Rise ($V_{CC}$ = 30 V, $I_C$ = 750 mA, $I_{B1}$ = 15 mA) | $t_r$ | − | − | 150 | ns |
| Storage ($V_{CC}$ = 30 V, $I_C$ = 750 mA, $I_{B1}$ = 15 mA) | $t_s$ | − | − | 525 | ns |
| Fall ($V_{CC}$ = 30 V, $I_C$ = 750 mA, $I_{B1}$ = 15 mA) | $t_f$ | − | − | 155 | ns |

4. Pulsed Condition: Pulse Width = 300 μsec, Duty Cycle ≤ 2%.
5. Guaranteed by design but not tested.

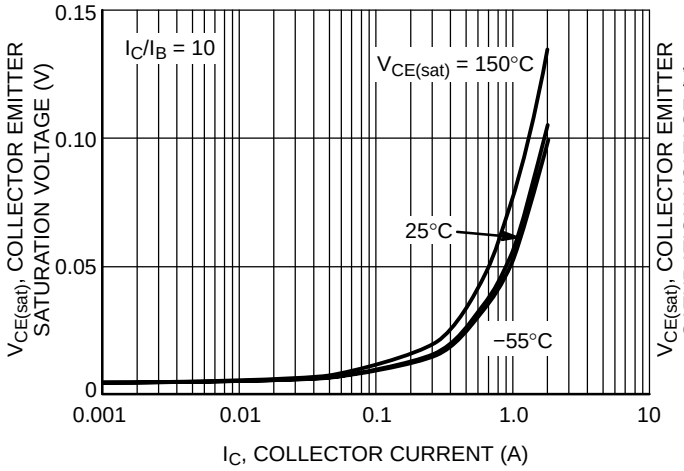



**Figure 1. Collector Emitter Saturation Voltage vs. Collector Current**

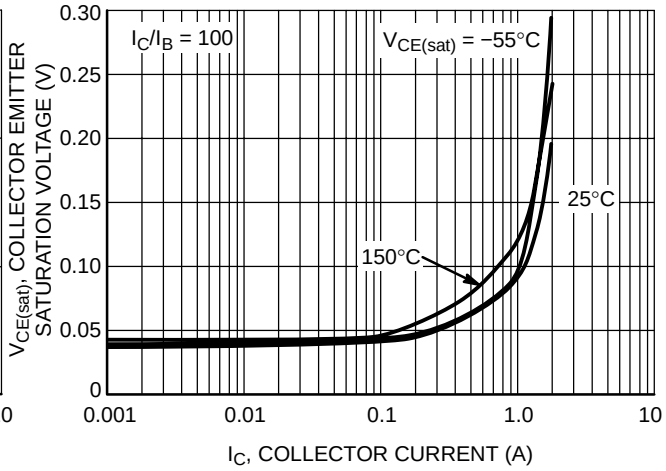



**Figure 2. Collector Emitter Saturation Voltage vs. Collector Current**

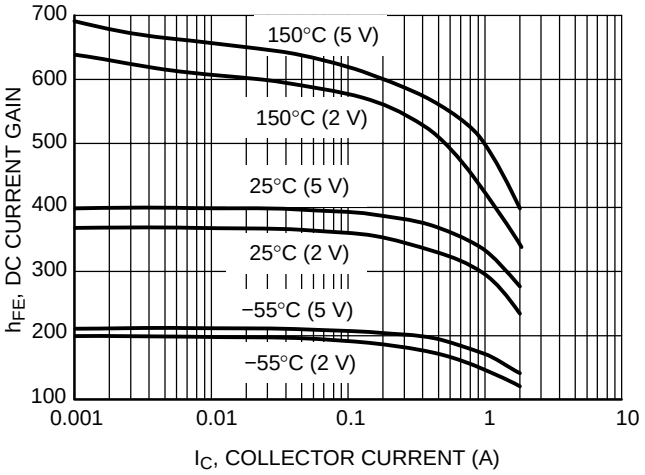



**Figure 3. DC Current Gain vs. Collector Current**

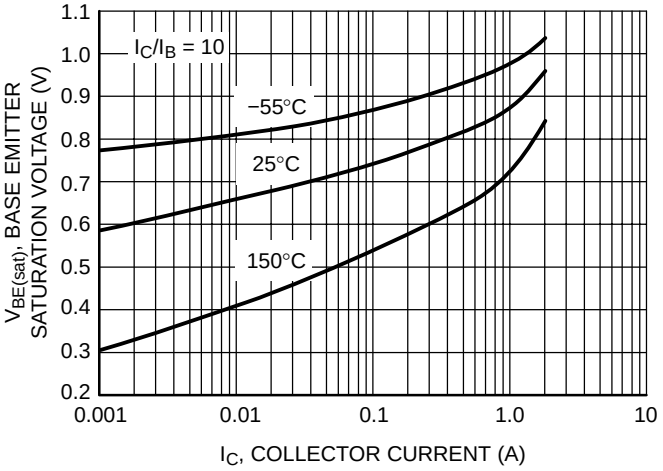



**Figure 4. Base Emitter Saturation Voltage vs. Collector Current**

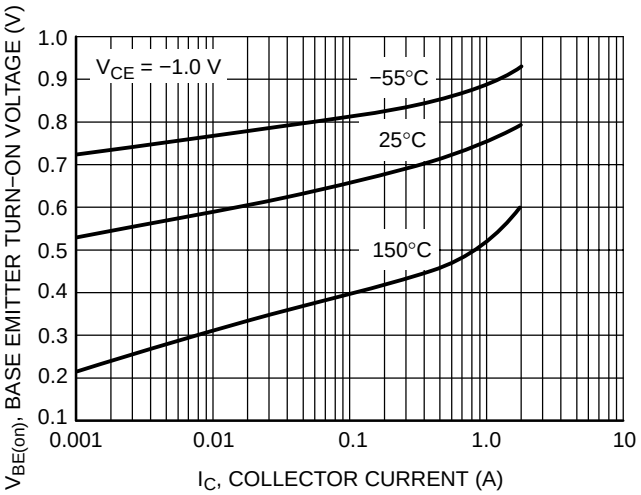



**Figure 5. Base Emitter Turn−On Voltage vs. Collector Current**

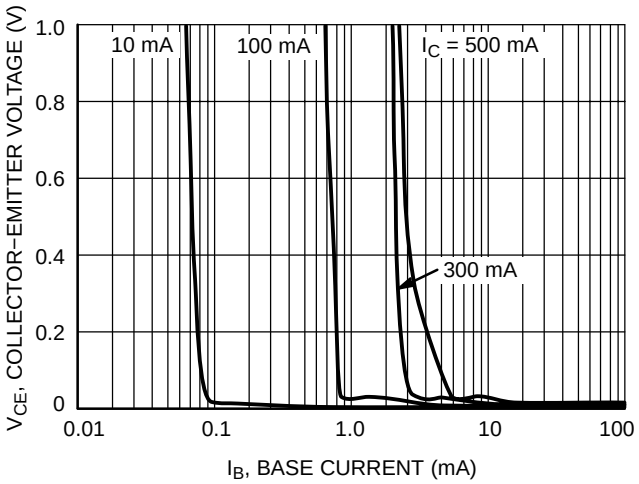



**Figure 6. Saturation Region**

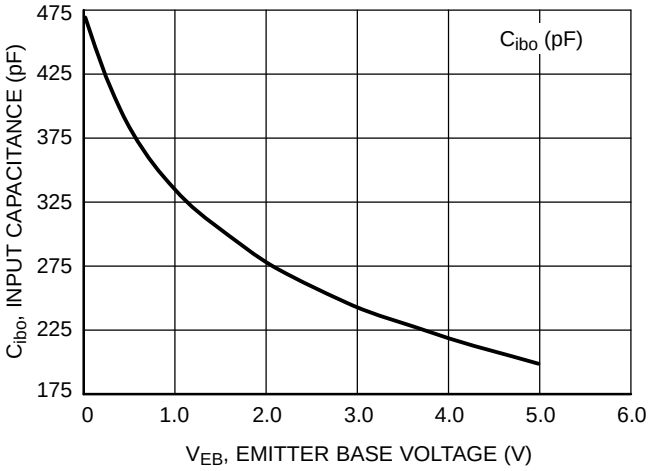



**Figure 7. Input Capacitance**

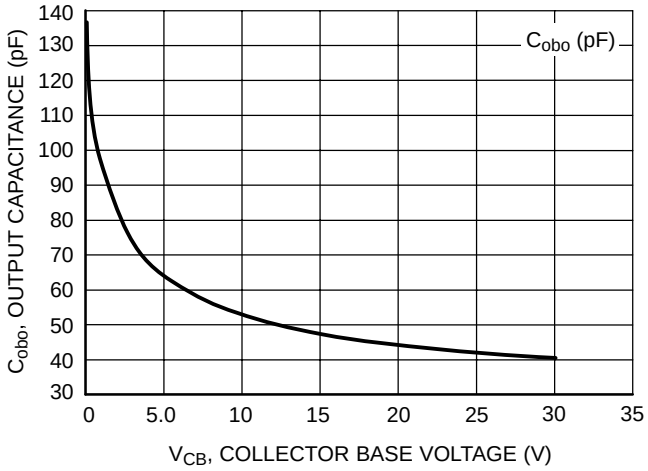



**Figure 8. Output Capacitance**

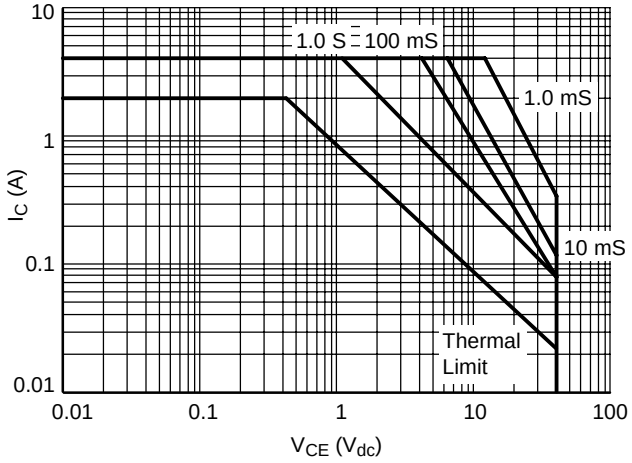
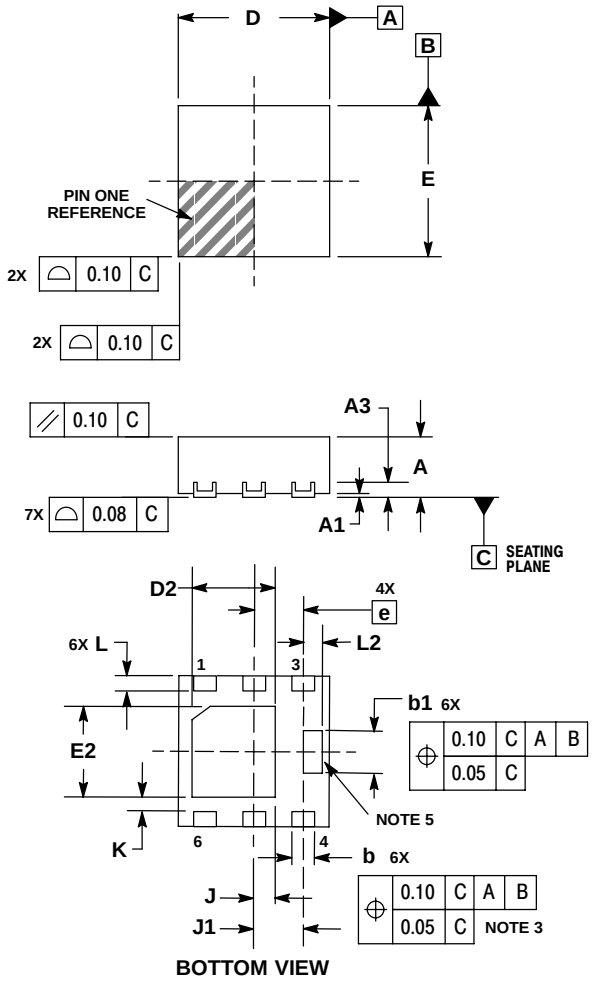



**Figure 9. PNP Safe Operating Area**

# NSS40200UW6T1G

## PACKAGE DIMENSIONS

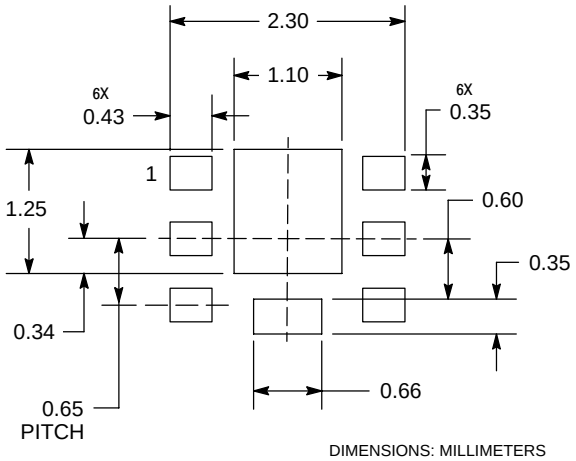
**WDFN6 2x2**
CASE 506AP−01
ISSUE B




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. CENTER TERMINAL LEAD IS OPTIONAL. TERMINAL LEAD IS CONNECTED TO TERMINAL LEAD # 4.
6. PINS 1, 2, 5 AND 6 ARE TIED TO THE FLAG.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.70 | 0.80 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.25 | 0.35 |
| b1 | 0.51 | 0.61 |
| D | 2.00 BSC | |
| D2 | 1.00 | 1.20 |
| E | 2.00 BSC | |
| E2 | 1.10 | 1.30 |
| e | 0.65 BSC | |
| K | 0.15 REF | |
| L | 0.20 | 0.30 |
| L2 | 0.20 | 0.30 |
| J | 0.27 REF | |
| J1 | 0.65 REF | |

**SOLDERING FOOTPRINT***




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



**PUBLICATION ORDERING INFORMATION**

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